# Semiconductor Fabrication Foundry

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**2009 Major IC Foundries**

| 2009 Rank | Company | Foundry Type | Location | 2007 Sales ($M) | 2008 Sales ($M) | 08/07 Sales % | 2009 Sales ($M) | 09/08 Sales % |
|---|---|---|---|---|---|---|---|---|
| 1 | TSMC | Pure-Play | Taiwan | 9,813 | 10,556 | 8% | 8,989 | -15% |
| 2 | UMC | Pure-Play | Taiwan | 3,430 | 3,070 | -10% | 2,815 | -8% |
| 3 | Chartered* | Pure-Play | U.S. | 1,458 | 1,743 | 20% | 1,540 | -12% |
| 4 | GlobalFoundries | Pure-Play | U.S. | 0 | 0 | N/A | 1,101 | N/A |
| 5 | SMIC | Pure-Play | China | 1,550 | 1,353 | -13% | 1,075 | -21% |
| 6 | Dongbu | Pure-Play | South Korea | 510 | 490 | -4% | 395 | -19% |
| 7 | Vanguard | Pure-Play | Taiwan | 486 | 511 | 5% | 382 | -25% |
| 8 | IBM | IDM | U.S. | 570 | 400 | -30% | 335 | -16% |
| 9 | SAMSUNG | IDM | South Korea | 355 | 370 | 4% | 325 | -12% |
| 10 | Grace | Pure-Play | China | 310 | 335 | 8% | 310 | -7% |
| 11 | He Jian | Pure-Play | China | 330 | 345 | 5% | 305 | -12% |
| 12 | Tower** | Pure-Play | Europe | 231 | 252 | 9% | 292 | 16% |
| 13 | HHNEC | Pure-Play | China | 335 | 350 | 4% | 290 | -17% |
| 14 | SSMC | Pure-Play | Singapore | 350 | 340 | -3% | 280 | -18% |
| 15 | TI | IDM | U.S | 450 | 315 | -30% | 250 | -21% |
| 16 | X-Fab | Pure-Play | Europe | 410 | 368 | -10% | 223 | -39% |
| 17 | MagnaChip | IDM | South Korea | 322 | 290 | -10% | 220 | -24% |

Source: IC Insights, company report

*Purchased by GlobalFoundries in 4Q09

**Tower bought Jazz in 2008

*Figure 1: 2009 Major IC Foundries (IC Insights, company report)*

Semiconductor Fabrication is the heart of the electronics supply chain, where the physical IC is fabricated and developed. The fabrication for a commercial product today requires processes that range between 300 and 900 steps, and takes 20 to 75 days depending on priority and intricacies. In today's global market most of the chips are fabricated on the wafer at 'pure play foundries', *Figure 1*. Pure play foundries sell unfinished IC-products into the supply chain, and operate as fabrication plants, producing ICs for other companies. Thus the challenges facing manufacturing flexibility in these foundries are more compared to the Integrated Device Manufacturer (IDM).

The continued effort to improve foundries is important since more and more IDM are moving towards foundries, including AMD, where its processors are now fabricated by Global Foundries. Another example is Intel's Atom chips being fabricated by TSMC.

In general, more than 10 active customers with more than 30 products are manufactured concurrently in a single pure play facility. A common goal for foundries is to meet the customer committed due date at the lowest cost. In order to ensure this goal is met, the manufacturing team is responsible to do appropriate planning and shop floor dispatching. The challenges include product types and where to process based on real time situation. The challenges are critical during high 'Work In Progress' and high mixed product. Other factors include differing due dates, varieties of product complexities, and temporary and planned bottlenecks.

Basic shop floor dispatching policies are First In First Out (FIFO), Shortest processing time (SPT), earliest due date (EDD), Shortest Remaining Cycle Time (SRPT) and also due date critical ratio (CR). Formulation for due date criticality (CR) is shown below:

CR = (Due Date – Current Time) / Standard Remaining Cycle Time

Further improvements to shop floor dispatching, maximizes utilization of bottlenecks by implementing 'hunger factors' to the bottleneck-equipment.

Hunger factor = Time required at bottleneck / Remaining time to bottleneck

Results of the effectives of using dispatching rules policies towards wafer fabrication has been established and the results might be different depending on the bottleneck equipment. A comparitive analysis will usually give different results based on foundry capacity setting and also process technology requirement. This is due to wafer fabrication requiring re-entrance processes that have

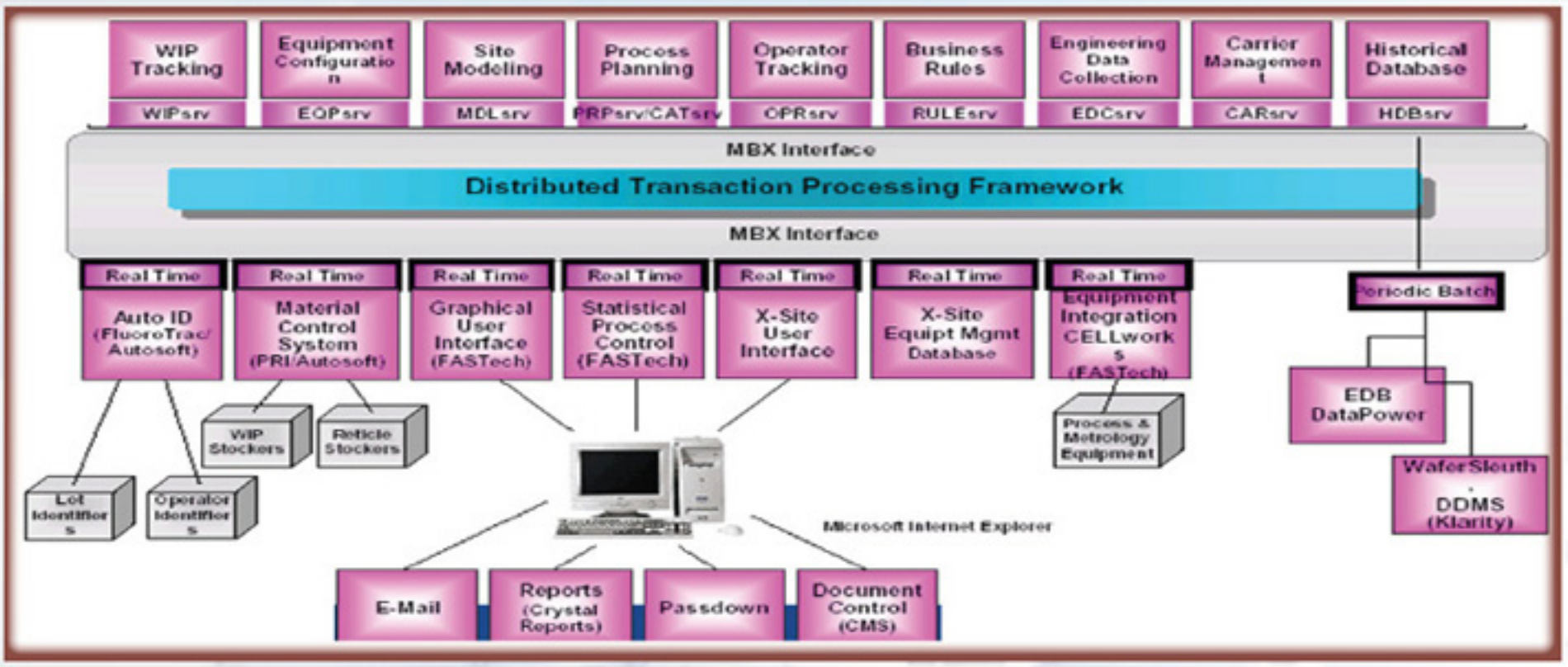
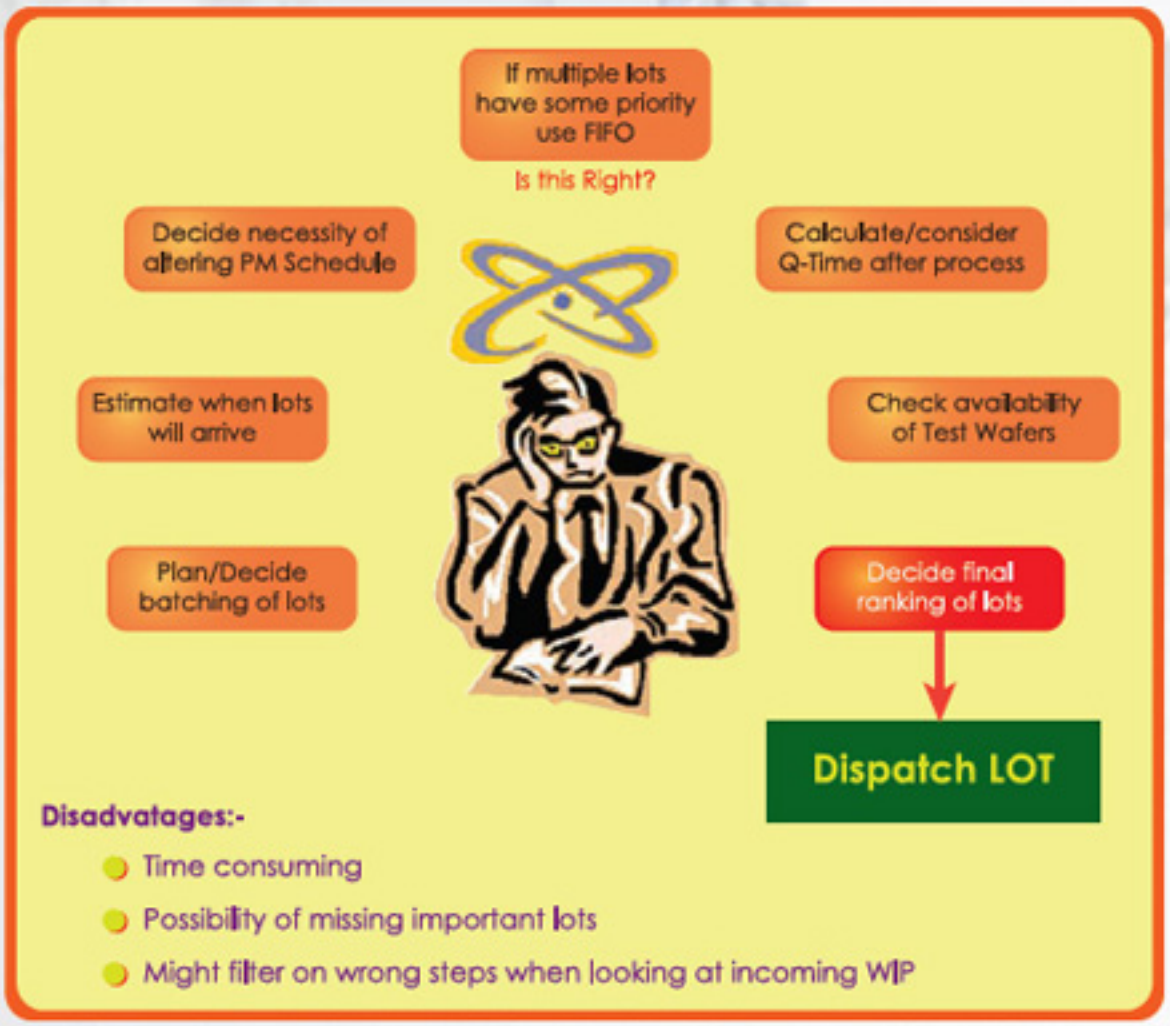



*Figure 2: Manufacturing Execution Systems (MES) using FactoryWorks (Brooks-PRI Automation 2002)*




*Which wafer product to select? (SilTerra Training for SilTerra Dispatching List (SDL))*

a mix of repeating at equipment. According to a recent publication from SilTerra Industrial Engineering Team and Institute Nano Electronic Engineering (INEE) UniMAP, the complexities include the processing steps that range from 300 to 900, and cycle times from 45 days to 90 days. The processes have a re-entrance to 90% of the equipment, with 30% re-entrance for 25 processing steps, followed by re-entrance for a range from 3 to 15 processing steps.

A strong analysis is required to cope with evolving and revolutionized dispatching approach to attack new problems caused by variability in the fabrication facility. All the variabilities are usually captured in the Manufacturing Execution Systems (MES) database. Examples of manufacturing execution systems used by semiconductor fabrication facilities are Factory Works, Promise, Workstream, 300Works, Fab300 and SiView. *Figure 2* illustrates, MES integration. List of variables that are traceable in MES and impact the shop floor dispatching includes:

1. Number of loading or order
2. Product and technology mix
3. Bottleneck Shift
4. Temporary bottleneck due to sporadic issues
5. Unscheduled maintenance for equipment due to internal and external cause
6. Customer priority and due date
7. Engineering prototyping
8. Quality related process time coupling, where next process need to be completed after current process at a stipulated time to avoid corrosion or other similar effects.

Once dispatching policies have been determined, a system wide calculation is needed to calculate the rank for each lot to weigh the priority accordingly.

## CONCLUSION

A review on the wafer fabrication operation shift from IDM to pure play has been presented with discussion on the arising challenges, and on the introduction to opportunities for potential solutions for optimization of overall customer due date commitment in high volumes. Basic solutions for scheduling and planning has been discussed. Further improvement for dispatching policies taking in account equipment bottleneck is made possible with hunger factors introduced. Overall manufacturing and operation personnel need to equip themselves with knowledge and know-how for computer systems' integration, in addition to applied mathematics for dispatch rule computation.

This artice is aimed at educating the lay-person in the intricacies of wafer fabrication